IN THE DRAWINGS

In Fig. 6, please change "520" to -- 520 -- as set forth in red on the separate letter to the Official Draftsperson.

IN THE CLAIMS

Please amend claims 6, 9, 11 and add new claims 14 and 15, so that these claims appear as follows.

6. (Amended) In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device;

using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device.

9. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

selectively grounding the body of at least one of the plurality of SOI devices to

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dissipate an electric charge accumulated in the body of the at least one of the plurality of SOI devices.

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11. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator connected to the circuit;

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using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator.

14. (New) A method for discharging accumulated charge from a body of an SOI device and accessing the SOI device, comprising:

generating a pulse;

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using the generated pulse to provide a conductive path from the body of the SOI device to a reference point having a lower potential than the accumulated charge;

discharging the accumulated charge from the body of the SOI device to the reference point;

providing a control signal which enables access to the SOI device; and

reading an output of the SOI device,

wherein said steps of generating a pulse and discharging the accumulated charge occur prior to said step of reading an output of the SOI device.

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15. (New) A method for reducing memory access time for a memory array which includes at least one SOI device, the method comprising:

activating a memory segment driver;

selecting a memory segment in the memory array;

generating a pulse in response to said selecting a memory segment;

connecting a select line to a ground potential in response to the generated pulse;

discharging any accumulated charge from a body of the at least one SOI device to the ground potential; and

accessing the selected memory segment after said discharging step.

REMARKS

Applicant amended claims 6, 9 and 11, and added new claims 14 and 15. Upon entry of this Amendment, claims 6-15 will be prosecuted in the present application.